

## CLAIMS

1. A semiconductor memory device comprising:

a plurality of memory cells (MC) arranged in a matrix; and

a gate line (GL), a word line (WL), a bit line (BL) and a source line

5 (SL), wherein

each of said plurality of memory cells (MC) includes:

a storage transistor (STr) having a first impurity region (22) and a  
second impurity diffusion region (24) opposed to each other through a first  
channel formation region (23a), a first gate electrode (19) formed above said  
10 first channel formation region (23a), and a charge accumulation node (23b)  
formed below said first channel formation region (23a); and

an access transistor (ATr) connected to said storage transistor (STr)  
in series, having said first impurity diffusion region (22), a third impurity  
diffusion region (20) opposed to said first impurity diffusion region (22)  
15 through a second channel formation region (21), and a second gate electrode  
(17) formed above said second channel formation region (21),

said second impurity diffusion region (24) is connected to said source  
line (SL), said third impurity diffusion region (20) is connected to said bit  
line (BL), said first gate electrode (19) is connected to said gate line (GL), and  
20 said second gate electrode (17) is connected to said word line (WL), and

by turning on/off said access transistor (ATr), a potential of said first  
impurity diffusion region (22) is switched to a fixed potential or a floating  
state, to thereby control the potential of said charge accumulation node (23b),  
and a threshold voltage of said storage transistor (STr) is thereby set at high  
25 level or low level.

2. The semiconductor memory device according to claim 1, wherein  
said threshold voltage of said storage transistor (STr) is set at high  
level by raising a potential of said first gate electrode (19) to high level from  
low level, with said access transistor (ATr) turned on, and

5 said threshold voltage of said storage transistor (STr) is set at low  
level, by raising the potential of said first gate electrode (19) to high level  
from low level, with said access transistor (ATr) turned off.

3. The semiconductor memory device according to claim 1, further  
comprising:

10 an SOI substrate (14) in which a semiconductor substrate (11), an  
insulating layer (12), and a semiconductor layer (13) are laminated in this  
order, wherein

said first to third impurity diffusion regions (22, 24, 20) and said first  
and second channel formation regions (23a, 21) are respectively formed in  
15 said semiconductor layer (13), and

said charge accumulation node (23b) is constituted as a part of said  
semiconductor layer (13).

4. The semiconductor memory device according to claim 1, further  
comprising:

20 a substrate on which a semiconductor substrate (50) of a first  
conductive type, a first well (51) of a second conductive type, and a second  
well (52) of said first conductive type are laminated in this order, wherein

said first to third impurity diffusion regions (60, 62, 58) and said first  
and second channel formation regions (61a, 59) are respectively formed in an  
25 upper surface of said second well (52), and

said charge accumulation node (61b) is constituted as a part of said second well (52).

5. The semiconductor memory device according to claim 1, further comprising:

5 a first memory cell (MCL) in which said threshold voltage of said storage transistor (STr) is set at high level;

a first reference bit line (RBL) connected to said first memory cell (MCL);

10 a second memory cell (MCH) in which said threshold voltage of said storage transistor (STr) is set at low level;

a second reference bit line (RBLH) connected to said second memory cell (MCH); and

a sense amplifier circuit that compares each potential of said first and second reference bit lines (RBL, RBLH) and the potential of the bit line (BL) connected to a reading memory cell (MC) serving as a reading object, and thereby detects whether said threshold voltage of said storage transistor (STr) provided in said reading memory cell (MC) is set at high level or low level.

6. The semiconductor memory device according to claim 5, wherein

20 said storage transistor (STr), said access transistor (ATr), a first transistor (Tr1), and a second transistor (Tr2) are sequentially connected in series from a power supply potential (VDD) side, between said power supply potential (VDD) and a ground potential (GND), and

25 each gate of said first and second transistors (Tr1 and Tr2) is connected to a drain of said first transistor (Tr1).

7. The semiconductor memory device according to claim 1, wherein  
when said threshold voltage of said storage transistor (STr) provided  
in a writing memory cell serving as a writing object is set at high level, the  
potential (GND) of low level is applied to a bit line (BL) connected to said  
5 writing memory cell, and when said threshold voltage of said storage  
transistor (STr) provided in said writing memory cell is set at low level, a  
writing circuit for applying the potential (VBL) of high level to said bit line  
(BL) connected to said writing memory cell is further provided.

8. The semiconductor memory device according to claim 1, further  
10 comprising:

an SOI substrate (14) in which a semiconductor substrate (11), an  
insulating layer (12), and a semiconductor layer (13) are laminated in this  
order, wherein

said SOI substrate (14) includes a memory cell array region formed  
15 with said plurality of memory cells (MC), and a peripheral circuit region  
formed with a peripheral circuit,

a first element isolation film (15) having a bottom face that is  
brought into contact with an upper surface of said insulating layer (12) is  
formed in said memory cell array region, and

20 a second element isolation film (140) having the bottom face that is  
not brought into contact with the upper surface of said insulating layer (12)  
is formed in said peripheral circuit region.

9. A semiconductor memory device which has a main surface formed  
with a first element isolation film (15) extending along a first direction,  
25 comprising:

a substrate (14) on which an element formation region (AR) extending along said first direction is defined by said first element isolation film (15);

a bit line (BL) extending along said first direction;

5 a plurality of gate lines (GL), a plurality of word lines (WL), and a plurality of source lines (SL), all extending along a second direction; and

a plurality of memory cells (MC) arranged side by side along said first direction in said element formation region (AR), wherein

said bit line (BL) is shared by said plurality of memory cells (MC),

10 and

one source line (SL) out of said plurality of source lines (SL) is shared by two memory cells (MC) which are adjacent to each other along said first direction out of said plurality of memory cells (MC).

10. The semiconductor memory device according to claim 9, wherein

15 said substrate (14) is an SOI substrate (14) in which a semiconductor substrate (11), an insulating film (12), and a semiconductor layer (13) are laminated in this order,

said SOI substrate (14) has a memory cell array region formed with said plurality of memory cells (MC) and a peripheral circuit region formed  
20 with a peripheral circuit,

said first element isolation film (15) has a bottom face that is brought into contact with an upper surface of said insulating layer (12), and

a second element isolation film (140) having a bottom face that is not brought into contact with the upper surface of said insulating layer (12) is  
25 formed in said peripheral circuit region.